REMARKS

In the Official Action mailed on **15 September 2006**, the Examiner reviewed claims 1-17. Restriction to one of the following inventions is required under 35 U.S.C. §121:

I. Claims 1-10, drawn to a method for solving constraints during functional verification, classified in class 716, subclass 5.

II. Claims 11-17, drawn to a method for image computation, classified in class 716, subclass 5.

Claims 1-8, and 10 were rejected under 35 U.S.C. §101, because the claimed invention is directed to non-statutory subject matter. Claims 1, 2, 7, 9, and 10 were objected to because of informalitites. Claims 1-10 were rejected under 35 U.S.C. §102(b) as being anticipated by Hulgaard et a. ("*Equivalence checking of combinational circuits using Boolean Systems*", IEEE Transactions on, Volume 18, Issue 7, Page(s) 903-917 hereinafter "Hulgaard").

Restriction requirement

Applicant confirms election of invention I without traverse. Claims 1-10 read on invention I. Claims 11-17 have been canceled without prejudice.

Objection to the Specification

Examiner recommended using proper language and format in the abstract.

Applicant has reformatted the abstract by merging paragraphs in the abstract into a single paragraph and has validated that the abstract does not exceed 150 words. No new matter has been added.

The disclosure is objected to because of the informalities.

Applicant has updated the information regarding a referenced Application related to the instant Application by providing its actual application number. No new matter has been added.

Rejection under 35 U.S.C. §101

Claims 1-8, and 10 were rejected under 35 U.S.C. §101, because the claimed invention is directed to non-statutory subject matter.

Applicant has corrected "an electromagnetic waveform" to "a computing environment" in both independent claims 1 and 10. A computing environment is a concrete, tangible, and useful subject matter. This correction finds support in page 31, lines 31-38 of the instant application, wherein it describes a computing environment that can be used to execute the constraint solving computer program, and wherein the computing environment can be a workstation computer.

No new matter has been added.

Claims 1, 2, 7, 9, and 10 were objected to because of informalities.

Applicant has replaced the unclear term "unioning" with "computing a union of" in claims 1, 2, 7, 9, and 10, which is the intended meaning of finding a "union" of a set of constraints.

No new matter has been added.

Rejections under 35 U.S.C. §102(b)

Claims 1-10 were rejected under 35 U.S.C. §102(b) as being anticipated by Hulgaard et al. ("*Equivalence checking of combinational circuits using Boolean Systems*", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 18, Issue 7, Page(s) 903-917, hereinafter "Hulgaard").

Applicant respectfully points out that Hulgaard teaches a technique for formally proving that two combinational circuits implement the same Boolean function (i.e., the two circuits are logically equivalent) (see Hulgaard, page 903 Introduction, first paragraph). This is directed to a formal equivalence checking problem in Electronic Design Automation.

In contrast, the instant application describes a technique for solving a set of random variables under a given set of constraints. More specifically, the

technique solves a following problem: for a set of "m" variables, $V = \{v_1, v_2, \ldots, v_m\}$, and a set of "$n$" relations or constraints, $C = \{ C_0, C_1, \ldots, C_n \}$, such that each constraint is a relation between expressions over a subset of the variables in V, solve the set of variables in V (see page 5, lines 9-13 of the instant application).

Applicant respectfully points out that the formal equivalence checking problem in Hulgaard and the constraint solving problem of the instant application are two distinct logic problems. Although both problems can be expressed in Boolean functions and further expressed in binary decision diagram (BDD) representations, the formal equivalence checking problem **compares the outputs** (variables) of two Boolean functions, whereas the constraint solving problem looks for solutions for a set of variables but **does not compare the values** for these variables.

Furthermore, the instant application describes a constraint solving technique that combines the following two consecutive operations: (A). *a conjunction of constraints* to generate a solution generator; and (B). *an existential quantification* of the variables in the solution generator to produce a new constraint. Combining these two operations is beneficial because a conjunction operation typically increases the size of a BDD representation, while an existential quantification operation typically decreases a BDD size. Therefore, by interleaving the application of these two operations, the technique can decrease the maximum size of the BDD representation that needs to be processed, whereby increases the size of the constraint set that can be solved, for a given level of computational resources (see page 5 line 26-29, to page 6, lines 1-6, and page 6, lines 14-29 to page 7, lines 1-25 of the instant application). The combination of these two operations has been presented in independent claims 1, 2, 9, and 10.

There is nothing within Hulgaard, either explicitly or implicitly, that suggests combining a conjunction of constraints to generate a solution generator, with an existential quantification of the variables in the solution generator, to produce a new constraint.

Hence, Applicant respectfully submits that independent claims 1, 2, 9, and 10 as presently amended are in condition for allowance. Applicant also submits that claims 3-8, which depend upon claim 2, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 
Shun Yao
Registration No. 59,242

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Shun Yao
PARK, VAUGHAN & FLEMING LLP
2820 Fifth Street
Davis, CA 95618-7759
Tel: (530) 759-1667
Fax: (530) 759-1665
Email: shun@parklegal.com